Progress Report

Grant #731009
Ultra-Efficient Generators & Diesel Electric Propulsion
Genesis Machining & Fabrication
Reporting Dates: 4/2013-6/2013

Deliverables Submitted:

UMIC Efficiency data.

Budget:

We are invoicing for $3,950.00 from grant funds for salary, $2,737.74 from grant funds for reimbursements, and $8,460.00 from grant funds in advance for electrical components and salary. We are submitting documentation of $14,850.00 in match for this period.

See attached files for receipt copies, receipt spreadsheet, invoices, request for advance payment, and match documentation.

Schedule Status:

We are slightly behind schedule in that we have not yet been able to measure the efficiency of our power dense motor. Working together with ACEP, we have developed a plan to make this measurement.

Percent Complete:

We are about 75% complete with the second milestone listed in the grant schedule. We have tested our TRL-6 UMIC for efficiency in our electric vehicle test-bed. Along with efficiency testing, we have demonstrated both the UMIC and the PDM in a working, drivable electric vehicle demonstration. An online video showing our working demonstration is available at: http://youtu.be/u9ae-Fyv_kI

Work Progress:

We have completed the following tasks during this quarter, and will review each in turn:

1) Fine-tuned inverter start-up sequence
2) Identified and tested a working fusing methodology for our inverter system
3) Designed, built, and tested a bottom balancing system for Li-Ion batteries
4) Implemented a working DC-DC output as one of the re-configurable outputs from the UMIC
5) RF noise amelioration and digital fault filtering
6) Developed a novel, high efficiency, IGBT switching algorithm
7) Did an initial thermal study of inverter core with ACEP
8) Calibrated inverter voltage and current sensing with ACEP
9) Gathered UMIC efficiency data

Inverter Start-up sequence

Safe start-up is important to inverter operation. Last quarter we had an IGBT failure during inverter start-up. After some forensic research we determined the failure cause. The FPGA can send non-deterministic (random, or high frequency) signals while booting. This can result in a dangerous condition leading to shoot-through currents and device failure. To protect against this, we have implemented a start-up sequence which involves fault-checks at each stage of inverter start-up. This start-up sequence has performed very well and has alerted us several times to potential failure conditions. Part of the start-up sequence involves pre-charging the inverter capacitors before connecting the main circuit. This prevents arcing in the main contact switches and contactor, and prevents the high speed fuses from blowing due to inrush currents.

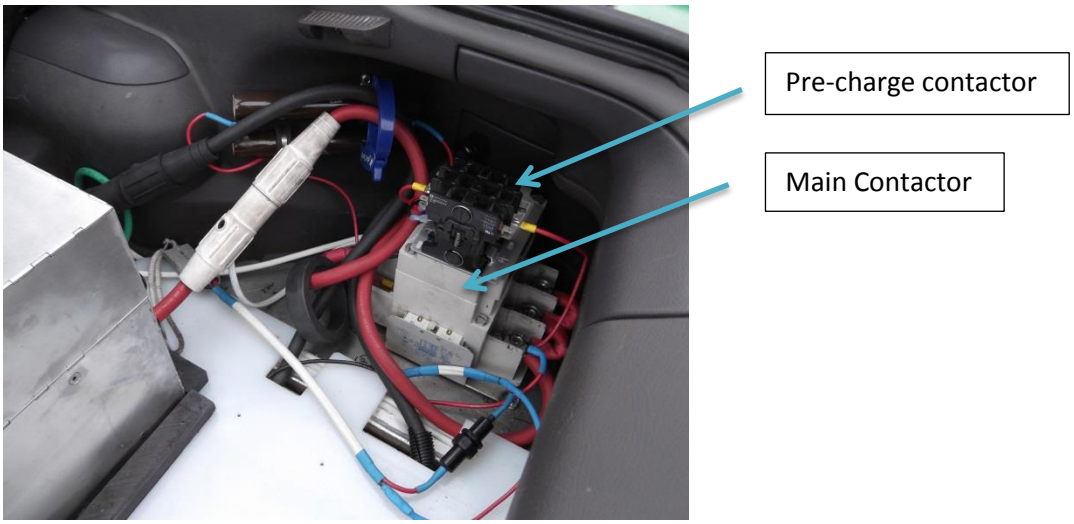

Figure 1 – Pre-charge and main contactors

Fusing Methodology

After more fuse research we have adopted a series of high speed semiconductor fuses from Mersen. We have a “test” fuse and a “drive” fuse in our EV testbed. The test fuse is used for tests related to drive algorithm, and the higher amperage drive fuse is for driving. These fuses have proven to be effective in preventing physical damage to the inverter during an actual device failure.

Battery Balancing System

A key component of many alternative energy systems is high density energy storage. In many marine applications lead-acid is still the chemistry of choice due

to familiarity and availability. However, the weight, low life expectancy, and low energy density of lead acid batteries render them impractical for high power applications such as marine auxiliary power or marine propulsion. Our EV testbed utilizes what we believe is one of the very best chemistries and cell technologies currently on the market – Lithium Iron Phosphate. Our LiFe cells are produced by Chinese Aviation Lithium Battery and are the cell of choice for many EV enthusiasts. The cells feature high power density, high C rating, and excellent thermal properties. Our EV pack comprises 118 cells at 60 AH each for a total pack with nearly 25 kWh of energy storage. One draw-back to all lithium chemistries is the need for careful balancing and management. Ultimately, the UMIC will need to support a variety of different battery management schemes. One common scheme used by the EV community is the bottom balance – all cells are discharged to a known SOC (state-of-charge) and then recharged such that the weakest cell does not exceed a chosen voltage threshold. We have developed both hardware and software for the UMIC to do bottom balancing for lithium batteries. We have successfully tested this system on our EV testbed battery.

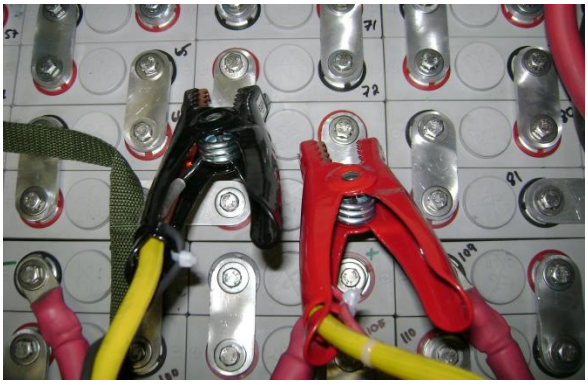

Figure 2 - Bottom balancing harness

DC-DC Converter Output

An important, novel aspect of the UMIC is its reconfigurable, generic outputs. One prototype feature we have tested in our EV is a programmable DC-DC converter. We did this because of the need for a 12 Volt supply from the inverter. Ideally a separate 12 volt DC-DC converter would be wired directly to the battery. However no DC-DC converters could be found to accept the 400 VDC from our battery. This problem will inevitably present itself in marine installations. To solve it, we programmed one of the reconfigurable outputs of the UMIC to output a DC

voltage of our choosing – in this case 150 VDC – and then used this voltage to power an off-the-self DCDC converter. This was a good working test of the UMIC's output flexibility.

RF Noise Amelioration

A problem we have been facing since the start of this project has been RF noise. This problem is particularly difficult in prototype situations where PCB's are not used. We performed a series of tests and while implementing various design changes and have significantly reduced the RF noise coming from the inverter and reduced the internal circuit's susceptibility to noise. The main technique used to reduce noise was placing common mode ferrites on all inverter outputs.

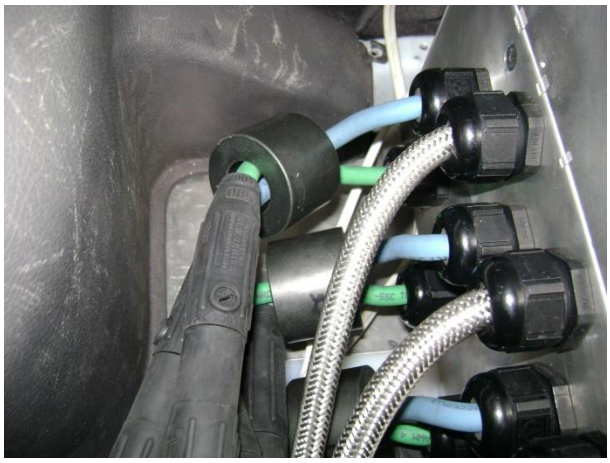

Figure 3 – Common mode ferrites

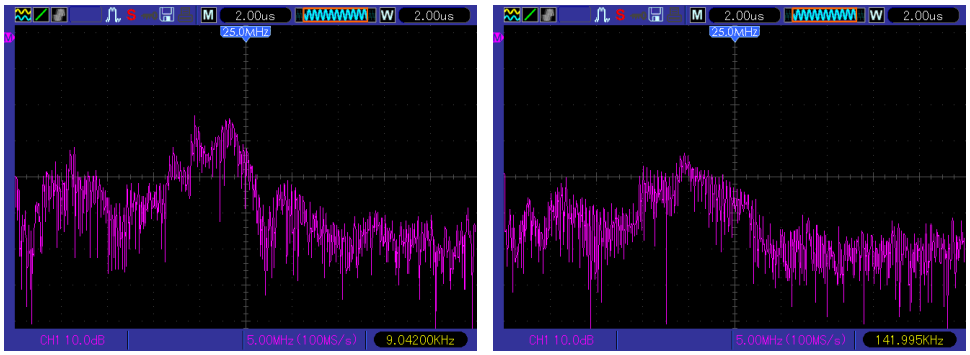

Figure 4 – Before and after FFT's showing a 10 dB Noise reduction

In addition to common mode noise filtering using ferrites, we have also implemented a digital filter to reject noise from the IGBT fault lines. We now believe that we have 100% noise rejection and see only bona fide fault signals.

We have tested this fault detection system to 2 us, which is five times faster than the recommended fault processing speed for our IGBT's.

High Efficiency Switching Algorithm

The source of inverter inefficiency is primarily to be found in switching losses. When semiconductors, such as IGBT's, are fully on, the losses are extremely low. However, as they are being switched between the off and the on state, they pass through a linear region where their losses become high. The key to increasing inverter efficiency is to reduce the amount of time spent switching. This can be done either by increasing the transition speed from off to on, reducing the PWM carrier frequency, or by using algorithms such as Space Vector Modulation (SVM) which yields incremental reductions in time spent switching.

In a standard three-phase inverter topology, using a PWM algorithm, all IGBT's are being switched all the time. Using our novel topology we have developed a PWM based switching scheme in which all IGBT's are switched only half of the time *when* the inverter output voltage is peak. At all other times, e.g. at lower than peak outputs, the time spent switching is further reduced, thus further increasing efficiency. Using this algorithm has yielded a measured inverter efficiency of 98% at 20kW. We believe further improvements are possible by adapting the SVM concept to the additional allowable switching vectors of our topology.

The drawback to this algorithm is that twice as many IGBT's are required. However, the reduced burden per switch and the higher efficiency probably make it a worthwhile tradeoff. We have successfully simulated this switching scheme using LabView / Multisim but have yet to do a formal efficiency comparison simulation.

Thermal Study

Using ACEP's FLIR camera system we performed a simple thermal study of key inverter components. The study supported our IGBT thermistor calibration, heat sink effectiveness, and the good thermal response of the power-ring film

capacitors. We hope to perform a more in-depth study in the future with inverter designs that can be viewed from the top while operating.

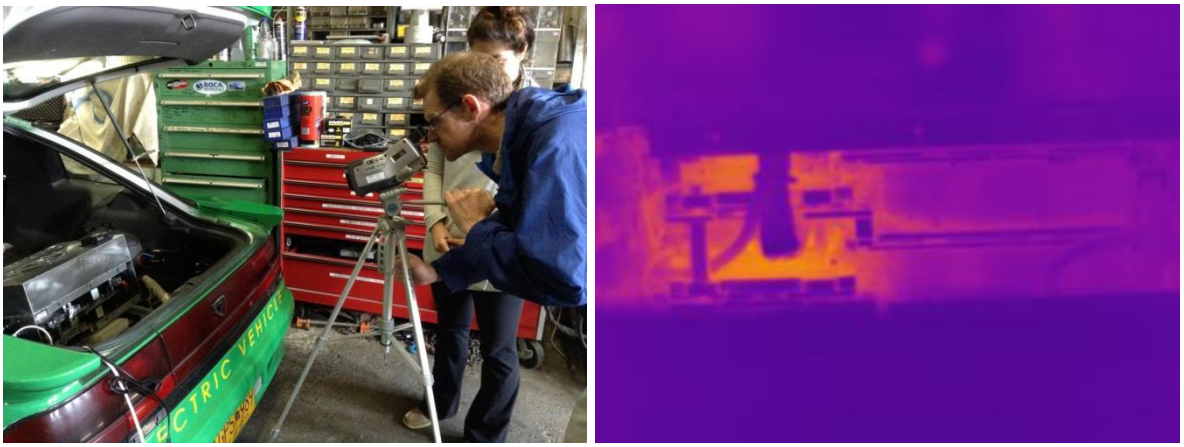

Figure 5 – (Left) Tom Johnson and Annie Goering of ACEP making FLIR picture of inverter and (right) photo of inverter layer under load

Voltage and Current Sensing Calibration

During a visit from Tom Johnson from ACEP, we calibrated the UMIC's voltage and current sensors and determined their degree of linearity. This voltage data is shown below. Current data was accepted by ACEP on site but not recorded.

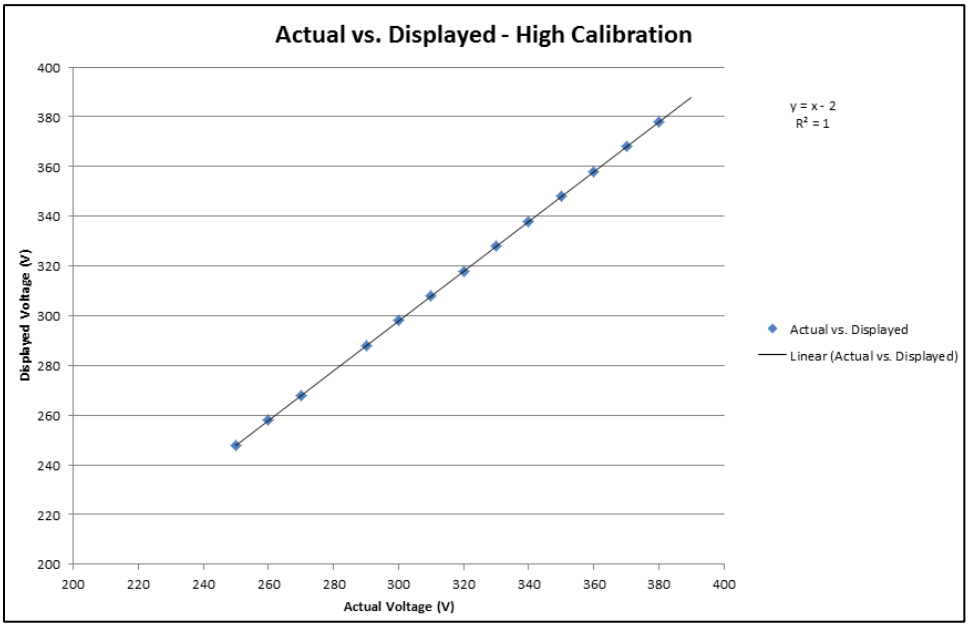

Figure 6 - Input side voltage calibration

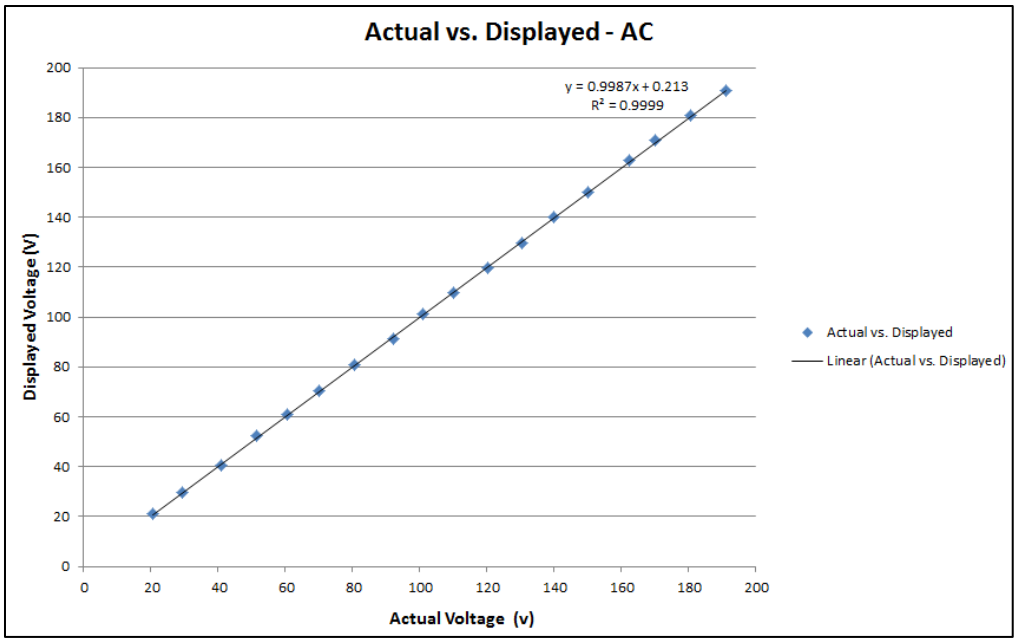

Figure 7 - AC Side Voltage Sensor Calibration

Another goal for this quarter was to measure PDM efficiency. We did not reach this goal because of lack of time. However, we did develop a plan with Mr. Johnson to approach the problem of measuring motor efficiency. ACEP will purchase a torque sensor which we will install on our bench motor. Then we will develop and test a motor efficiency measurement algorithm against measured efficiency. Once this algorithm is calibrated, we will use it to develop a power curve for our installed EV PDM.

UMIC Efficiency Data

An efficiency curve was developed by lifting the front end of the EV on jack-stands and running the car in forth gear while pressing the brake. Data points represent averages of 200 samples. This test was limited to 20kW because of excessive brake temperatures. At 20 kW the peak measured efficiency was 98.1%. We are working with ACEP to identify third party equipment to corroborate our measurements.

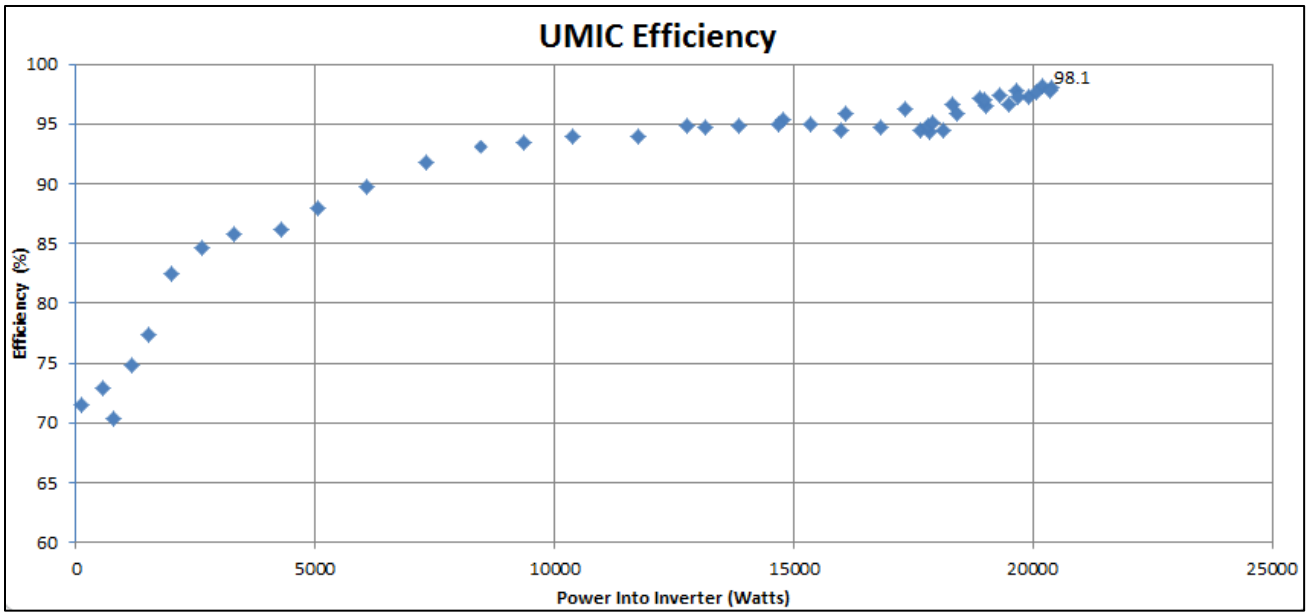

Figure 8 - Efficiency curve developed with vehicle on test-stand

Another efficiency plot was generated under actual driving conditions. We limited this test run to under 30 kW for several reasons which we will explain in the next section.

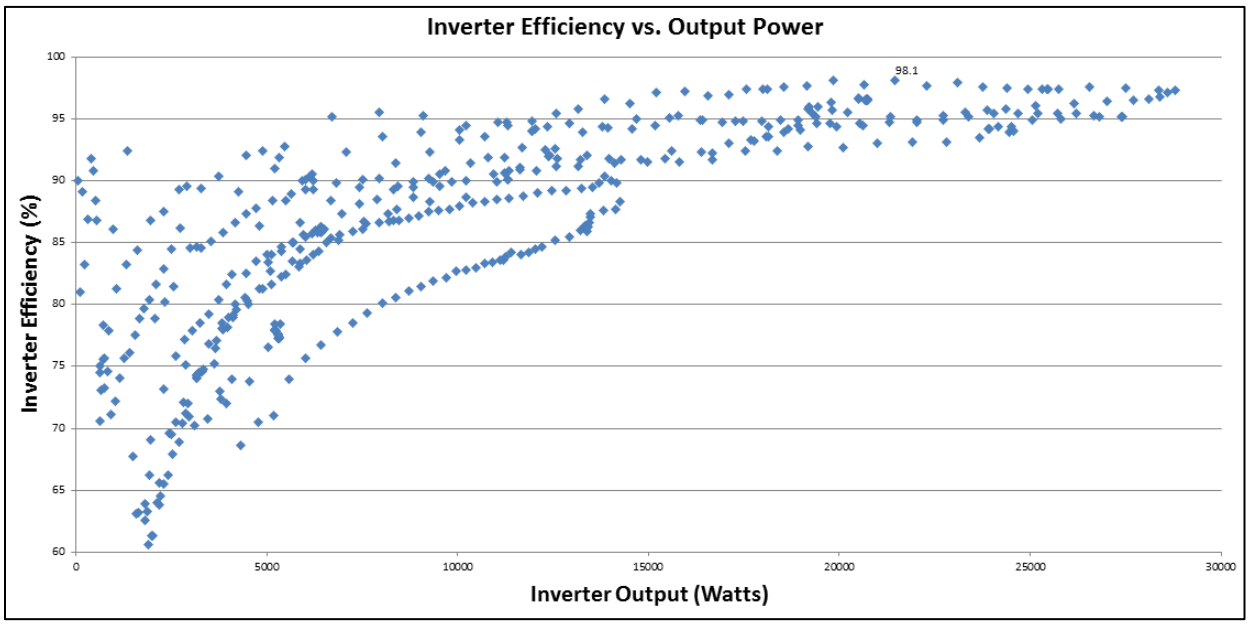

Figure 9 - Efficiency curve developed while driving EV

Each test yielded a peak efficiency of 98.1%. During testing it was noted that peak efficiencies occurred once steady-state conditions had been reached. At this time it is not known if this is a function of the inverter itself or of the measurement

technique. However, we believe that it has to do with measurement because efficiency was calculated on the non-deterministic side of the data flow chain, and this would cause sections of waveforms to be unaccounted for during acceleration. While the peak efficiencies of the envelope should be believed, the lower efficiencies may in fact be artifacts of measurement technique. We are hoping to move the efficiency metering algorithm to the FPGA to circumvent this limitation.

We also found a strong correlation between IGBT temperature and inverter efficiency. For the range studied in this experiment efficiency *increased* with temperature.

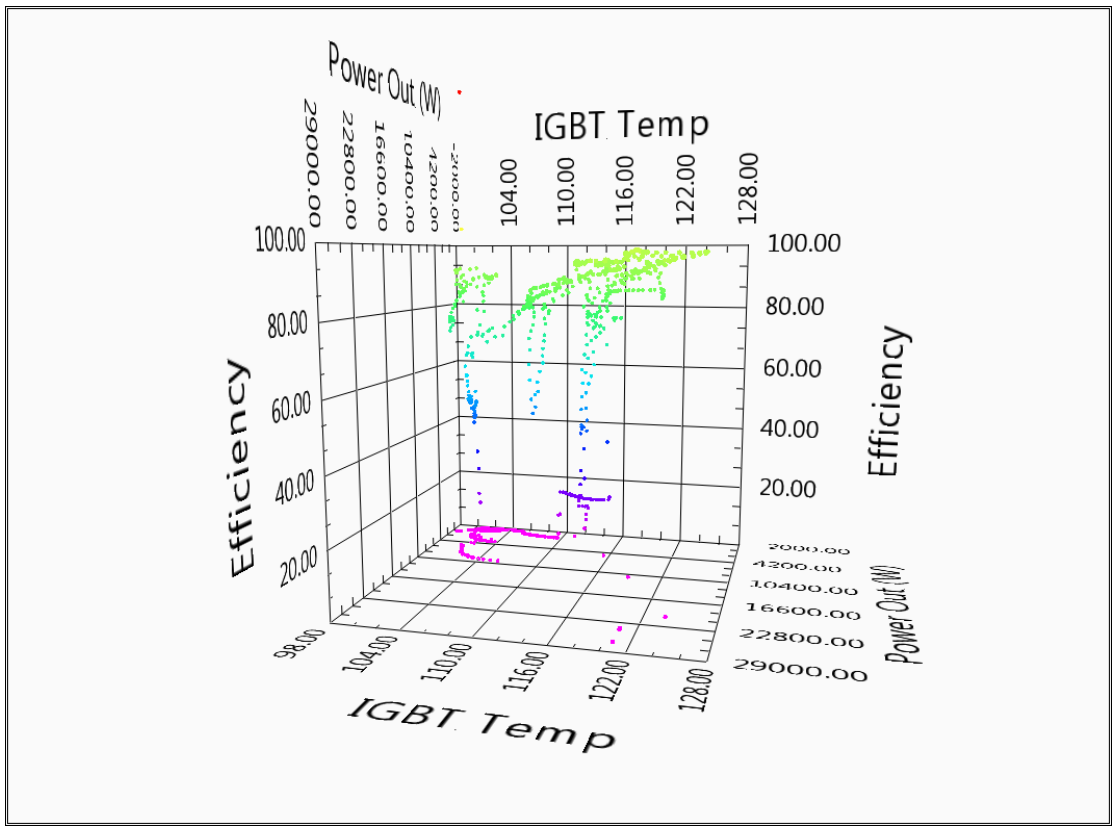

Figure 10 - 3D Scatter plot of IGBT Temperature, Inverter Power, and Efficiency

As can be seen from the plot there are three distinct clusters of data points. Each cluster represents a different acceleration period during the test drive, and during consecutive periods the inverter temperature had risen. The efficiencies are highest when the temperature was highest, in this case 120°F. In future studies

we will try to determine a peak efficiency temperature and develop an algorithm to maintain that temperature.

Limitations to Full Power Testing.

We are currently limiting our power testing to less than 30 kW due to two weak links in our power chain: failing IGBT's and clutch vibration. In our last report we described a failure event during which an IGBT suffered a shoot-through condition due to FPGA instability during boot-up. At the time it seemed that only one unit was affected, however further testing is revealing that other units are also damaged and unable to perform at full power. We are in the process of ordering a new set of IGBT's to fix this problem. Additionally, our stock clutch is vibrating above 5k RPM and therefore limiting peak output. We have obtained a racing clutch and flywheel and will be installing it soon.

Once these repairs are made we are confident that we can begin power testing above 100kW.

Other Notes from ACEP's Visit

The following items were discussed during ACEP's site visit:

1. Acquiring a diesel fuel flow meter to assist in our genset efficiency study.
2. Acquiring a torque sensor to calibrate our motor efficiency measurement algorithm
3. Identifying equipment to make accurate current and or power measurements on inverters to confirm our measurements.

Work for Next Quarter

1. Full load testing

   Once we have made repairs to our inverter and clutch we will log data at higher loads.

2. PDM Efficiency Testing

As previously stated, we will be borrowing a torque meter from ACEP to calibrate our measurement algorithm. Once this is done we will develop an efficiency map of our Power Dense Motor.

3. 15kW Load-Matching Genset
   This is the major task at hand for next quarter. We will be using our TRL-6 inverter in conjunction with a 15 kW genset in a load matching configuration and begin data collection.

4. PCB Design

   Another task which we will be starting this quarter is the design of the TRL-7 UMIC. One of the major design tasks for this project is the printed circuit board design. Prof. Steven Bitar from Worcester Polytechnic Institute in Worcester, Mass. will be travelling to Kodiak later this summer with an intern to make a rough draft of the design. Then he will have a group of senior electrical engineering students design, build, and test the boards as a project to fulfill their graduation requirements.